PATENT ABSTRACTS OF JAPAN

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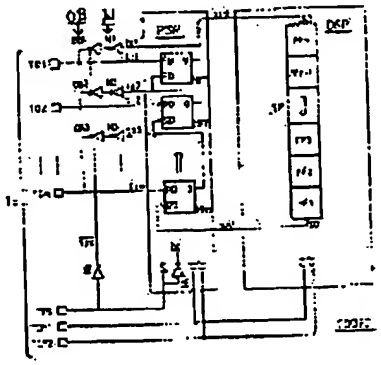
(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:

PURPOSE: To reduce the cost for a test by providing a parallel-series conversion register which sends test data to a scan path in series and also sends it to a testing device, and matching the number of bits with the bit constitution of a test pattern memory.

CONSTITUTION: The m-bit test input data ti1 - tim are supplied to parallel input terminals PD of FF circuits MF1 - MFm which constitute the parallel- series conversion register PSR from the testing device TE through corresponding test data input/output terminals TD1 - TDm. Further, uninverted output signals Q of precedent circuits MF2 - MFm are supplied to serial input terminals SD of the circuits MF1 - MFm-1. Scan-out data sod is supplied from the scan path SP to the terminal SD of the circuit MFm. The uninverted output signals Q of the circuits MF1 - MFm are further sent out to the device TE as test output data to1 - tom through corresponding inverter circuits N, output buffers OB, and terminals TD1 - TDm.



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